

INTEL'S TRI-GATE TRANSISTOR TO ENABLE NEXT ERA IN ENERGY EFFICIENT PERFORMANCE

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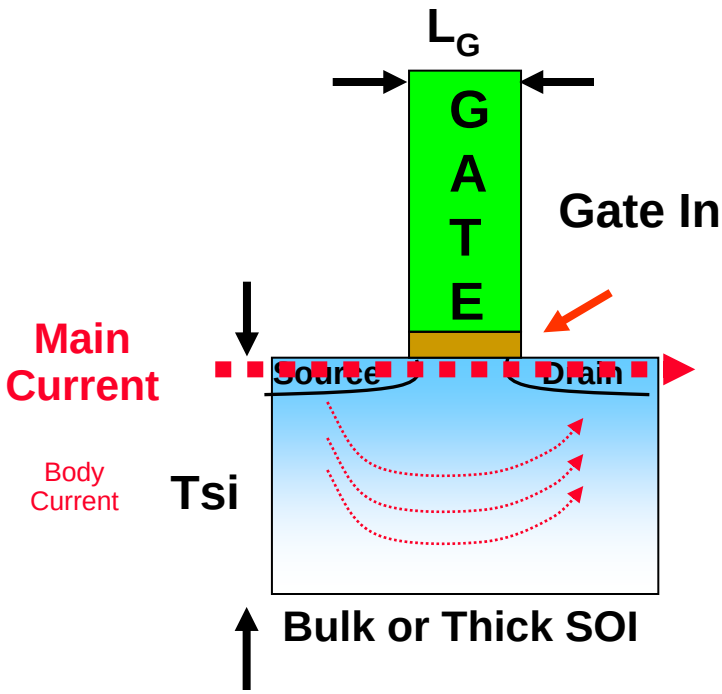
June 2006

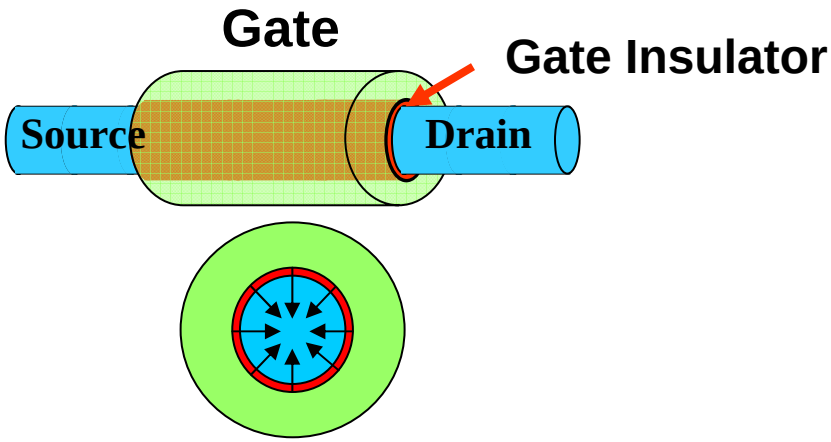


Overview

- Intel has demonstrated improved CMOS tri-gate transistors; these make use of high-k gate dielectrics, metal gate electrodes, and strained silicon
- Intel was first to demonstrate these individual pieces and has now successfully integrated them together
- These transistors are a critical part of Intel's energy efficient performance philosophy; they offer considerably lower leakage and consume much less power than today's planar transistors

Improving on a Planar Transistor

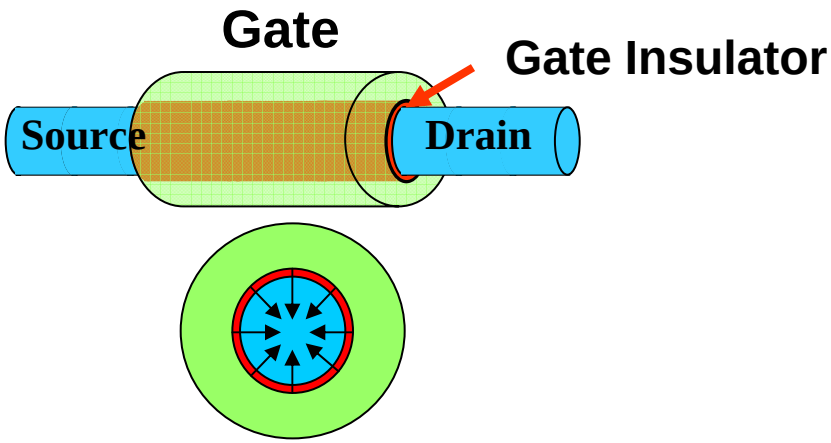


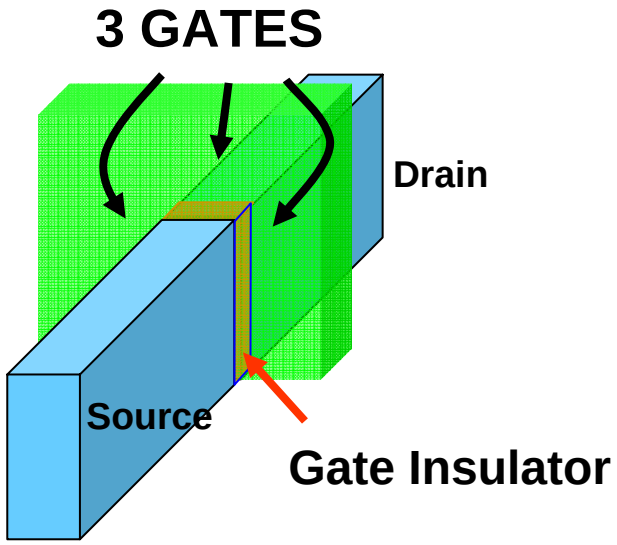


- In planar devices on-current is mostly carried in a thin top layer
- Body current is a source of leakage when the device is off

- An ideal transistor would have a gate surround a very thin channel
- This gives the highest on to off ratio & therefore highest power efficiency

Tri-gate: Surrounding the Channel

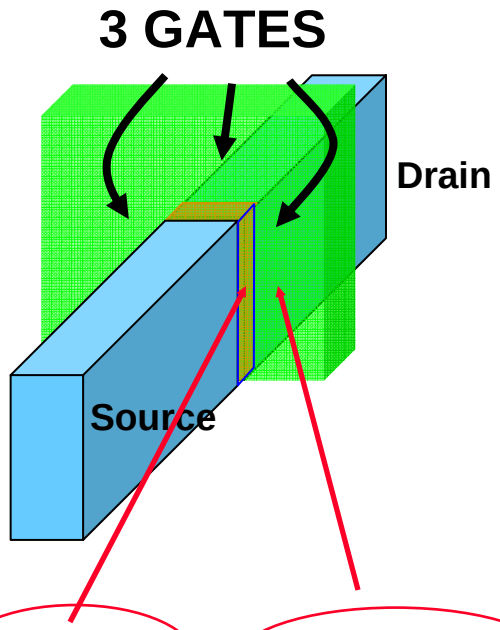




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1. The tri-gate surrounds the channel on three of four sides
- It is significantly better than both Planar and FinFET
- This geometry alone though isn't enough …

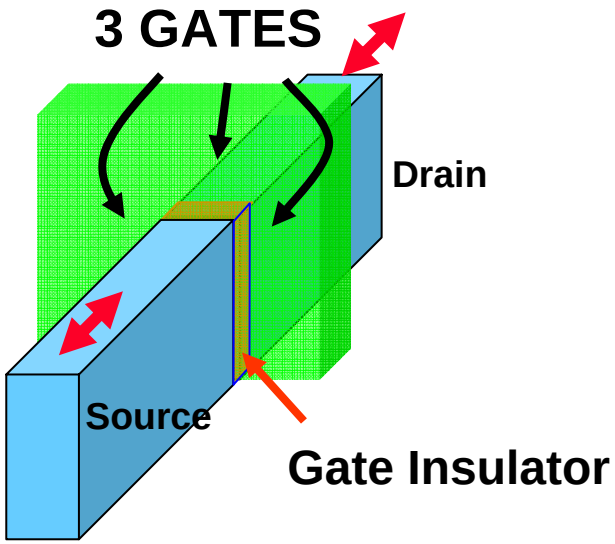
Optimizing even Further



2. Using high-k and metal gates improves both on and off current

- Faster & cooler operation !

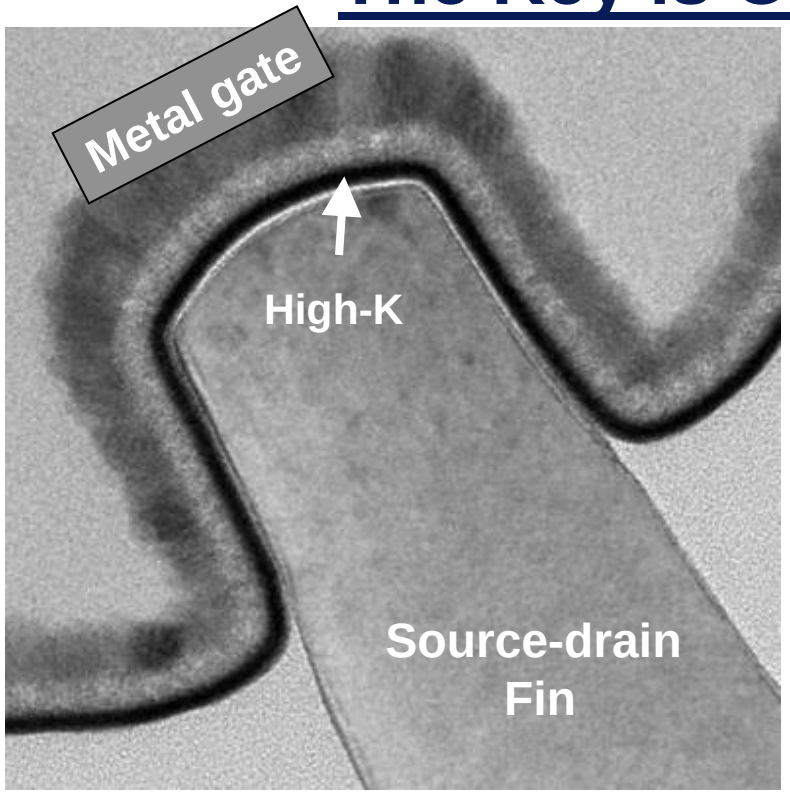
Squeeze the PMOS
Stretch the NMOS

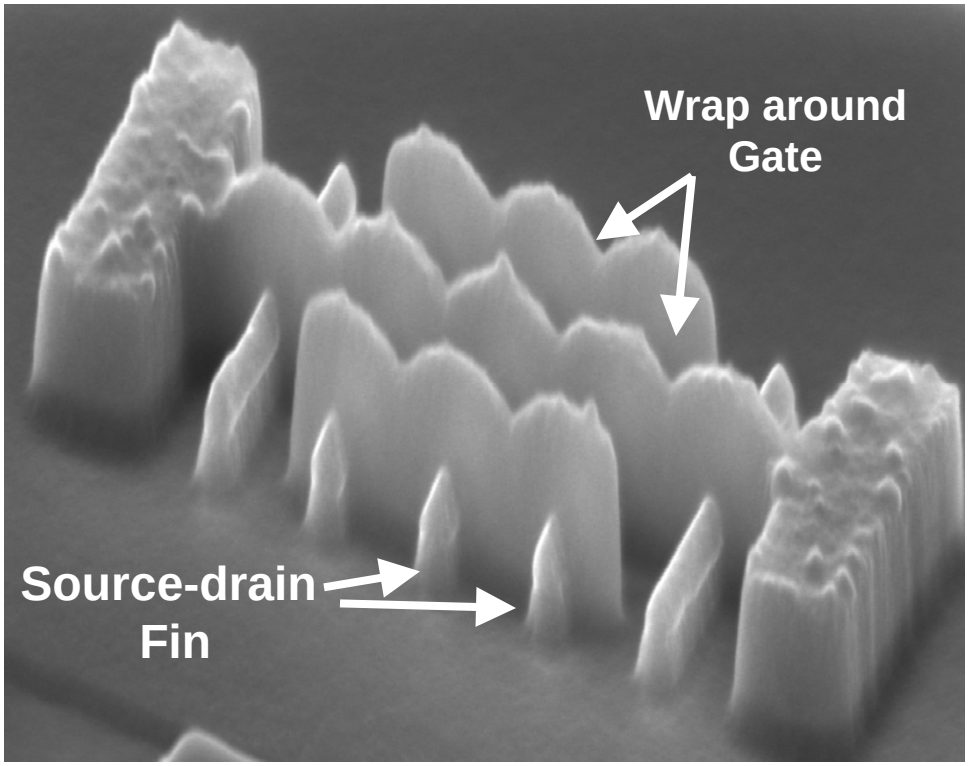


3. Adding strain improves the mobility = better performance

- Faster & cooler operation !

The Key is Optimizing the Integration





1. **Tri-gate gives better off current and therefore less wasted power**
2. **High k – metal gate gives both higher speed and less wasted power**
3. **Strained Si produces higher speed and less wasted power**

The sum of all these pieces is once again world leading transistors

Intel Tri-gate Summary

- Compared to today's world leading 65nm transistors, this integrated tri-gate transistor can offer
 - 45% increase in speed or 50x reduction in off-current
 - 35% reduction in total power at constant speed
- These results demonstrate Intel's leadership in integrated processes as we have successfully integrated three key elements – tri-gate geometry, high-k dielectrics, and strain -- to once again produce record drive currents and transistor efficiency
- Intel expects that these transistors could become the basic building blocks for future microprocessors sometime beyond the 45nm node
- While this is one of several options under investigation, these results give us high confidence that we can continue Moore's Law scaling well into the next decade

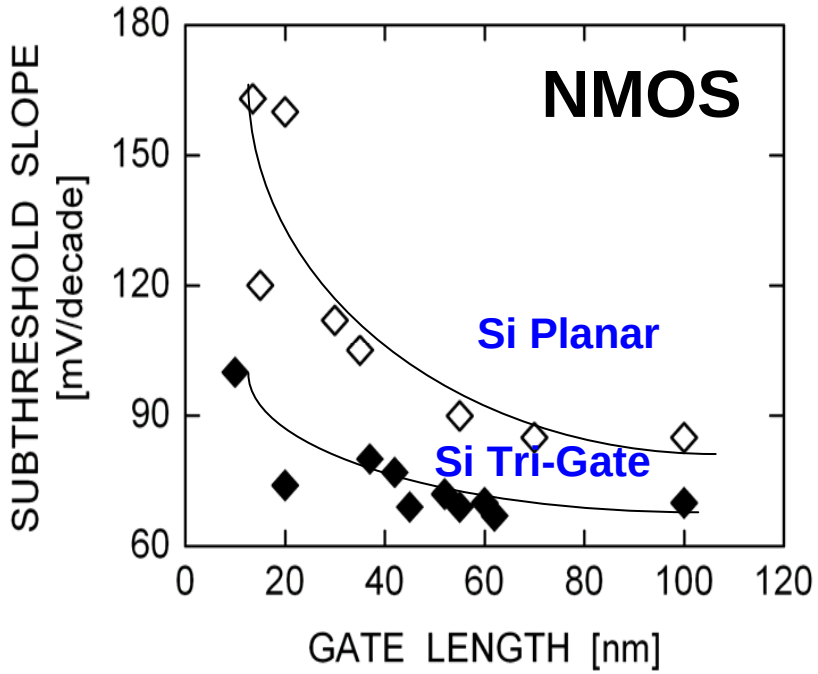


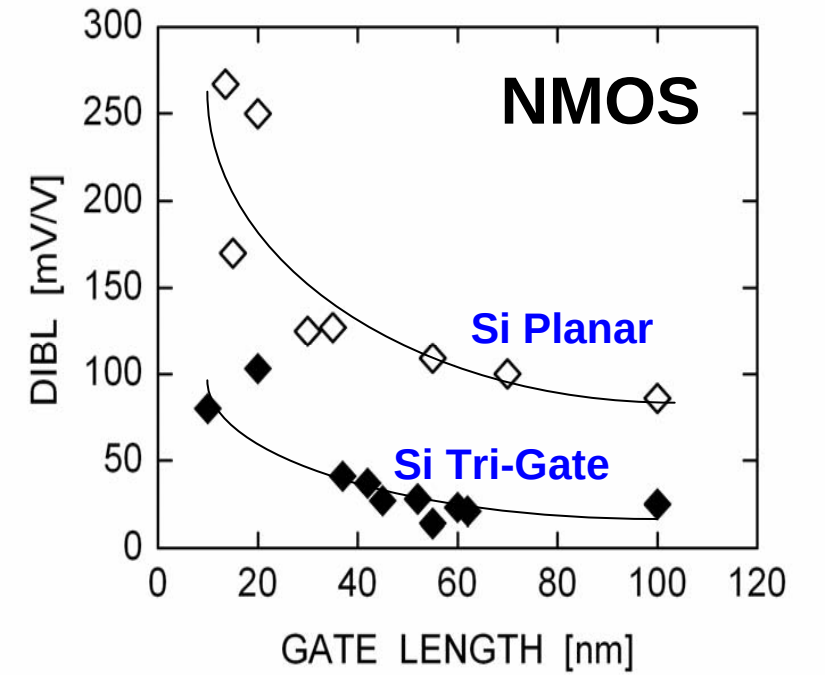
Details to be presented at the 2006 Symposium on VLSI Technology in Honolulu, Hawaii

Session 7 - June 13th

"Tri-Gate Transistor Architecture with high-K gate Dielectrics, Metal Gates, and Strain Engineering"
Jack Kavalieros et al.

Tri-gate Shows Improved Scalability Over Planar Devices





Tri-Gate transistors provide better short-channel-effects control which enable continued gate length (L_G) scaling over planar Si devices